ABSTRACT:

A data processing device, for example, an MPEG decoder, comprises a bus system [BUS] over which a transmitter circuit, for example a variable length decoder circuit [VLD], can transfer a series of samples to a receiver circuit, for example, an IS circuit. The transmitter circuit is arranged for transmitting only a start of the series of samples which extends up to a point where the samples that are left are equal to a reference value and for transmitting an indication "end of transmission" after the last transmitted sample. The receiver circuit is arranged for placing reference values after the sample preceding the indication "end of transmission", so as to reconstitute the series of samples.

Fig. 1.